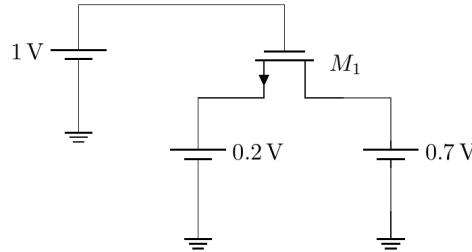


Question 1

Determine the region of operation of M_1 . Identify the source and calculate V_{GS} and V_{DS} . Express the classification in terms of V_{TH} and justify the inequalities.



Detailed solution

The device is an NMOS. The terminal at the lower potential is the source: the 0.2 V terminal. The other terminal is the drain, and the gate is at 1 V.

$$V_S = 0.2 \text{ V}, \quad V_D = 0.7 \text{ V}, \quad V_G = 1 \text{ V}$$

Calculate the two controlling voltages. For an enhancement NMOS, conduction requires V_{GS} greater than the threshold.

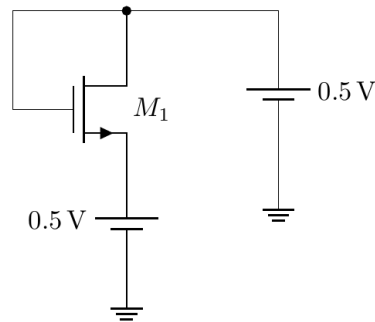
$$V_{GS} = 0.8 \text{ V}, \quad V_{DS} = 0.5 \text{ V}, \quad V_{OV} = 0.8 - V_{TH}$$

Compare V_{DS} with the overdrive. The threshold is not specified, so the answer is conditional; 0.3 V is the triode/saturation boundary. For example, a 0.4 V threshold gives saturation.

$$\begin{cases} \text{cutoff,} & V_{TH} \geq 0.8 \text{ V}, \\ \text{saturation,} & 0.3 \text{ V} \leq V_{TH} < 0.8 \text{ V}, \\ \text{triode,} & V_{TH} < 0.3 \text{ V}. \end{cases}$$

Question 2

Determine the region of operation of M_1 . Calculate the terminal voltages and justify whether the device is off, in triode, or in saturation. State any required threshold assumption.



Detailed solution

Both channel terminals and the gate are at 0.5 V. With equal channel potentials, choosing either channel terminal as the source gives the same result.

$$V_G = V_D = V_S = 0.5 \text{ V}, \quad V_{GS} = V_{DS} = 0$$

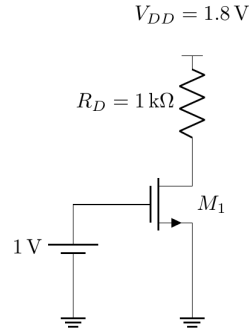
For the usual enhancement device with a positive threshold, V_{GS} is below threshold: the device is off and I_D is zero in the ideal model.

$$V_{TH} > 0 \implies \text{cutoff}, \quad I_D = 0$$

If the threshold were negative, a channel would exist but V_{DS} would still be zero, so its ideal drain current would remain zero (the zero- V_{DS} triode limit). At zero threshold the device is at threshold.

Question 3

Assume $\lambda = 0$. Find W/L for M_1 at the edge of saturation, with $V_{DD} = 1.8\text{ V}$, $R_D = 1\text{ k}\Omega$, and $V_G = 1\text{ V}$. Express the result in terms of V_{TH} and $\mu_n C_{ox}$.



Detailed solution

The source is grounded, so V_{GS} is 1 V . At the edge of saturation the drain voltage equals the overdrive.

$$V_{DS} = V_{OV} = 1 - V_{TH}, \quad V_D = 1 - V_{TH}$$

Apply Ohm's law to R_D , then use the square-law saturation current with λ equal to zero.

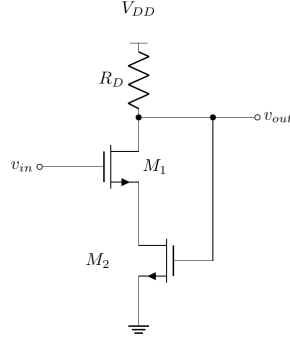
$$I_D = \frac{1.8 - (1 - V_{TH})}{R_D} = \frac{0.8 + V_{TH}}{R_D} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (1 - V_{TH})^2$$

Solving for geometry gives the symbolic design. Voltages in the expression are in volts. It requires a positive overdrive and a positive drain current. As an illustration only, $V_{TH}=0.4\text{ V}$ and $\mu_n C_{ox}=200\text{ microA/V squared}$ give $I_D=1.2\text{ mA}$ and $W/L=33.3$.

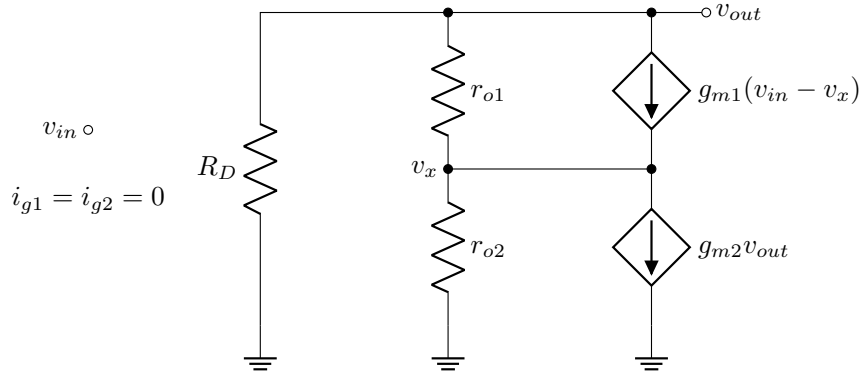
$$\boxed{\frac{W}{L} = \frac{2(0.8 + V_{TH})}{R_D \mu_n C_{ox} (1 - V_{TH})^2}}, \quad -0.8 < V_{TH} < 1$$

Question 4

Construct the complete small-signal equivalent circuit. Assume both transistors operate in saturation with $\lambda \neq 0$. Include g_{m1} , g_{m2} , r_{o1} , and r_{o2} . Label the input, output, and internal node; ignore body effect.



Detailed solution



Replace VDD with AC ground. Let v_x be the junction of the source of M1 and drain of M2. The drain of M1 is v_{out} ; the source of M2 is grounded. The gate of M1 is v_{in} , while the gate of M2 is connected to v_{out} .

$$v_{gs1} = v_{in} - v_x, \quad v_{gs2} = v_{out}$$

For M1, place r_{o1} between v_{out} and v_x and a controlled current source from v_{out} to v_x . For M2, place r_{o2} from v_x to ground and a controlled source from v_x to ground. R_D connects v_{out} to AC ground. Both gate currents are zero; body effect is ignored.

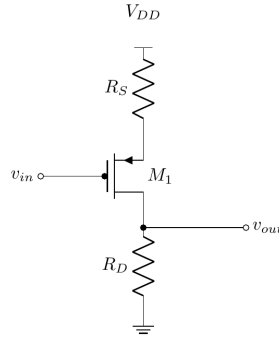
$$i_{d1} = g_{m1}(v_{in} - v_x) + \frac{v_{out} - v_x}{r_{o1}}, \quad i_{d2} = g_{m2}v_{out} + \frac{v_x}{r_{o2}}$$

The following two node equations fully specify the equivalent circuit. Do not ground the signal input: only independent DC supplies become AC ground.

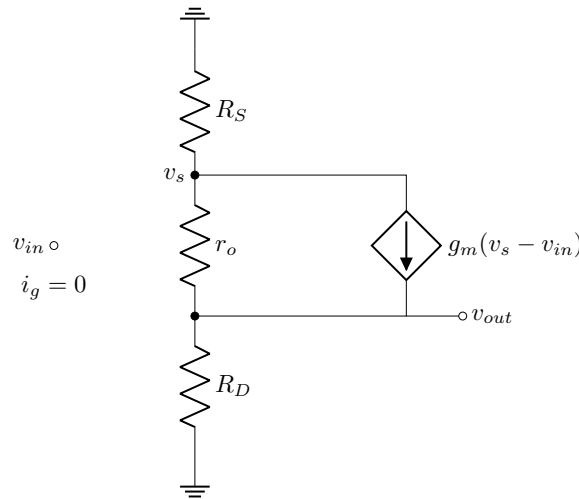
$$\frac{v_{out}}{R_D} + \frac{v_{out} - v_x}{r_{o1}} + g_{m1}(v_{in} - v_x) = 0, \quad \frac{v_x - v_{out}}{r_{o1}} - g_{m1}(v_{in} - v_x) + \frac{v_x}{r_{o2}} + g_{m2}v_{out} = 0$$

Question 5

Construct the complete small-signal equivalent circuit. Assume M_1 operates in saturation with $\lambda \neq 0$. Replace the DC supply with AC ground; include the controlled source, output resistance, and both resistors. Label input and output; ignore body effect.



Detailed solution



Replace VDD with AC ground, keeping R_S from the source node v_s to ground and R_D from the drain/output node to ground. The PMOS gate is driven by v_{in} and draws no current.

$$v_{sg} = v_s - v_{in}, \quad i_g = 0$$

Use a positive g_m magnitude. The PMOS controlled source points from source to drain with value $g_m(v_s - v_{in})$, and r_o lies between the same two nodes. This convention makes the signs explicit.

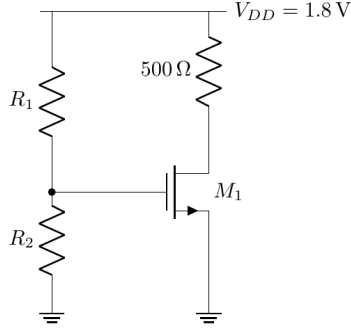
$$i_{s \rightarrow d} = g_m(v_s - v_{in}) + \frac{v_s - v_{out}}{r_o}$$

Write KCL at the source and drain. These equations, together with the drawing, are the complete small-signal model including finite output resistance.

$$\frac{v_s}{R_S} + \frac{v_s - v_{out}}{r_o} + g_m(v_s - v_{in}) = 0, \quad \frac{v_{out}}{R_D} + \frac{v_{out} - v_s}{r_o} - g_m(v_s - v_{in}) = 0$$

Question 6

Unless otherwise stated: $\mu_n C_{ox} = 200 \mu\text{A}/\text{V}^2$, $\mu_p C_{ox} = 100 \mu\text{A}/\text{V}^2$, $V_{TH,n} = 0.4 \text{ V}$, $V_{TH,p} = -0.4 \text{ V}$, and $\lambda = 0$. Design the gate-bias network for a drain current of 1 mA. For $W/L = 20/0.18$, determine R_1 and R_2 such that the input resistance is at least $20 \text{ k}\Omega$.



Detailed solution

Use the process values given in the question. The square-law current determines the required gate voltage because the source is grounded.

$$\beta = \mu_n C_{ox} \frac{W}{L} = 22.222 \text{ mA}/\text{V}^2, \quad V_{OV} = \sqrt{\frac{2I_D}{\beta}} = 0.3 \text{ V}, \quad V_G = 0.4 + 0.3 = 0.7 \text{ V}$$

Since the gate draws no DC current, the divider ratio fixes R_1/R_2 . Its parallel resistance is the input resistance. Choose the smallest allowed input resistance for a concrete design; multiplying both resistors by any factor at least one is also valid.

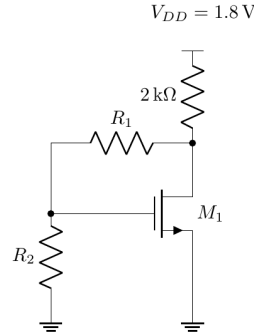
$$\alpha = \frac{V_G}{V_{DD}} = \frac{7}{18}, \quad R_1 = \frac{R_{in}}{\alpha}, \quad R_2 = \frac{R_{in}}{1 - \alpha}$$

At $R_{in} = 20 \text{ k}\Omega$, the following values meet both requirements. The drain resistor carries only transistor current; the transistor is in saturation.

$$\boxed{R_1 = 51.43 \text{ k}\Omega, \quad R_2 = 32.73 \text{ k}\Omega}, \quad V_{DS} = 1.8 - (1 \text{ mA})(500 \Omega) = 1.3 \text{ V} > 0.3 \text{ V}$$

Question 7

Unless otherwise stated: $\mu_n C_{ox} = 200 \mu\text{A}/\text{V}^2$, $\mu_p C_{ox} = 100 \mu\text{A}/\text{V}^2$, $V_{TH,n} = 0.4 \text{ V}$, $V_{TH,p} = -0.4 \text{ V}$, and $\lambda = 0$. Design the stage for a transistor drain current of 0.5 mA . For $W/L = 50/0.18$, determine R_1 and R_2 such that the current through these resistors is one-tenth of I_{D1} .



Detailed solution

First find the gate voltage for a transistor current of 0.5 mA . The divider current is fixed at one-tenth of the transistor current.

$$\beta = 55.556 \text{ mA}/\text{V}^2, \quad V_{OV} = \sqrt{\frac{2(0.5 \text{ mA})}{\beta}} = 0.13416 \text{ V}, \quad V_G = 0.53416 \text{ V}, \quad I_B = 50 \mu\text{A}$$

The $2 \text{ k}\Omega$ drain resistor supplies both the transistor and divider currents. Including that extra current is essential when calculating V_D .

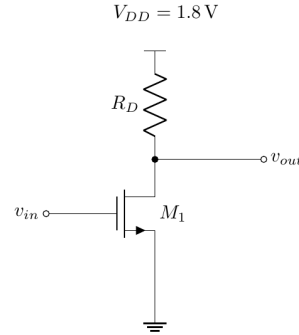
$$V_D = 1.8 - (I_D + I_B)(2 \text{ k}\Omega) = 0.7 \text{ V}$$

R_1 is between drain and gate; R_2 is between gate and ground. Ohm's law now gives the design. Finally V_{DS} exceeds the overdrive, confirming the assumed saturation region.

$$\boxed{R_1 = \frac{V_D - V_G}{I_B} = 3.317 \text{ k}\Omega, \quad R_2 = \frac{V_G}{I_B} = 10.683 \text{ k}\Omega, \quad 0.7 > 0.13416}$$

Question 8

Unless otherwise stated: $\mu_n C_{ox} = 200 \mu\text{A}/\text{V}^2$, $\mu_p C_{ox} = 100 \mu\text{A}/\text{V}^2$, $V_{TH,n} = 0.4 \text{ V}$, $V_{TH,p} = -0.4 \text{ V}$, and $\lambda = 0$. Design the common-source stage for a voltage-gain magnitude of 5, subject to $W/L \leq 20/0.18$. Determine the required R_D if the power dissipation must not exceed 1 mW.



Detailed solution

The constraints are upper bounds, so the design is not unique. Choose both maximum allowed current and maximum W/L to give one concrete solution (and the smallest R_D within these bounds).

$$I_D = \frac{P_{max}}{V_{DD}} = \frac{1 \text{ mW}}{1.8 \text{ V}} = 0.55556 \text{ mA}, \quad \frac{W}{L} = \frac{20}{0.18} = 111.111$$

With lambda zero and the source grounded, the gain is minus $g_m R_D$. Compute the transconductance and set the gain magnitude to five.

$$g_m = \sqrt{2\mu_n C_{ox}(W/L)I_D} = 4.9690 \text{ mS}, \quad \boxed{R_D = \frac{5}{g_m} = 1.0062 \text{ k}\Omega}$$

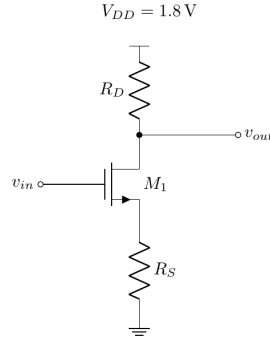
Check the DC drain voltage against the overdrive. The required gate voltage is approximately 0.6236 V. The current and geometry limits and the saturation condition are all satisfied. Other smaller allowed currents/geometries may also work with a correspondingly larger R_D .

$$V_{OV} = \frac{2I_D}{g_m} = 0.22361 \text{ V}, \quad V_D = 1.8 - I_D R_D = 1.24098 \text{ V} > V_{OV}, \quad A_v = -5$$

Question 9

Unless otherwise stated: $\mu_n C_{ox} = 200 \mu\text{A}/\text{V}^2$, $\mu_p C_{ox} = 100 \mu\text{A}/\text{V}^2$, $V_{TH,n} = 0.4 \text{ V}$, $V_{TH,p} = -0.4 \text{ V}$, and $\lambda = 0$. The source-degenerated common-source stage must provide a voltage-gain magnitude of 4 at a bias current of 1 mA. The DC voltage drop across R_S is 200 mV, and $\lambda = 0$.

(a) For $R_D = 1 \text{ k}\Omega$, determine the required W/L . Does the transistor operate in saturation for this choice? (b) For $W/L = 50/0.18$, determine the required R_D . Does the transistor operate in saturation for this choice?



Detailed solution

The specified DC drop sets R_S . With no channel-length modulation or body effect, source degeneration gives the following gain.

$$R_S = \frac{0.2 \text{ V}}{1 \text{ mA}} = 200 \Omega, \quad A_v = -\frac{g_m R_D}{1 + g_m R_S}$$

Part (a): solve for g_m with $R_D = 1 \text{ k}\Omega$ and gain magnitude four. Then use g_m squared divided by twice the process parameter and current to determine W/L .

$$g_m = \frac{4}{R_D - 4R_S} = 20 \text{ mS}, \quad \boxed{\frac{W}{L} = \frac{g_m^2}{2\mu_n C_{ox} I_D} = 1000}, \quad V_{OV} = 0.1 \text{ V}$$

The drain is at 0.8 V and source at 0.2 V, so $V_{DS} = 0.6 \text{ V}$ exceeds the overdrive. Part (a) is in saturation.

$$V_{DS,a} = 1.8 - (1 \text{ mA})(1 \text{ k}\Omega) - 0.2 = 0.6 \text{ V} > 0.1 \text{ V}$$

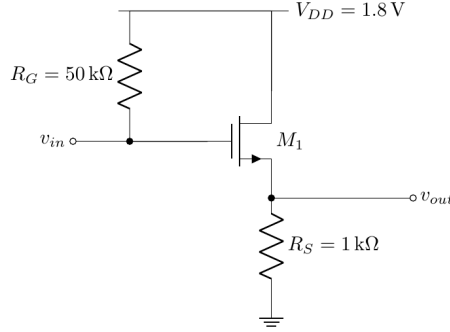
Part (b): calculate g_m for the specified geometry, then solve for R_D . Check saturation with the new drain voltage. Both choices yield a gain of minus four.

$$g_m = 10.5409 \text{ mS}, \quad \boxed{R_D = 4 \left(\frac{1}{g_m} + R_S \right) = 1.17947 \text{ k}\Omega}$$

$$V_{OV} = 0.18974 \text{ V}, \quad V_{DS,b} = 0.42053 \text{ V} > V_{OV}$$

Question 10

Unless otherwise stated: $\mu_n C_{ox} = 200 \mu\text{A}/\text{V}^2$, $\mu_p C_{ox} = 100 \mu\text{A}/\text{V}^2$, $V_{TH,n} = 0.4 \text{ V}$, $V_{TH,p} = -0.4 \text{ V}$, and $\lambda = 0$. The source follower is biased through R_G . Determine its small-signal voltage gain v_{out}/v_{in} for $W/L = 20/0.18$ and $\lambda = 0.1 \text{ V}^{-1}$. Ignore body effect.



Detailed solution

The gate draws no DC current, so R_G sets $V_G = V_{DD} = 1.8 \text{ V}$. Let I denote the drain current in amperes. The source voltage is $1000 I$; the gate-source overdrive and drain-source voltage follow.

$$V_S = 1000I, \quad V_{OV} = 1.4 - 1000I, \quad V_{DS} = 1.8 - 1000I, \quad \beta = 22.222 \text{ mA}/\text{V}^2$$

Use the square-law model including the stated nonzero λ in the DC current as well as the small-signal parameters. Select the physical root with positive overdrive.

$$I = \frac{\beta}{2}(1.4 - 1000I)^2 [1 + 0.1(1.8 - 1000I)] \implies I_D = 1.09638 \text{ mA}$$

Thus $V_S = 1.09638 \text{ V}$, $V_{OV} = 0.30362 \text{ V}$, and $V_{DS} = 0.70362 \text{ V}$; saturation is valid. Differentiate the same current model to obtain g_m and g_{ds} . Using $r_o = 1/(\lambda I_D)$ is a common approximation; the expression below keeps the λ factor consistently.

$$g_m = \beta V_{OV}(1 + \lambda V_{DS}) = 7.22194 \text{ mS}, \quad g_{ds} = \frac{\lambda I_D}{1 + \lambda V_{DS}} = 0.10243 \text{ mS}, \quad r_o = 9.7627 \text{ k}\Omega$$

At AC the drain is grounded, so r_o and R_S both load the source. KCL gives the source-follower gain. R_G affects input resistance, not the gain from the stated gate voltage v_{in} .

$$g_m(v_{in} - v_{out}) = \left(g_{ds} + \frac{1}{R_S}\right) v_{out}, \quad \boxed{\frac{v_{out}}{v_{in}} = \frac{g_m}{g_m + g_{ds} + 1/R_S} = 0.86757}, \quad R_{in} = R_G = 50 \text{ k}\Omega$$